Amendments to the Claims

Listing of Claims - This will replace all prior listings of claims in the application:

1. (Currently Amended) An apparatus, comprising:

- a clock source to generate a clock signal;

- a first circuit, coupled to a first supply voltage source, to generate a first data signal and a second circuit coupled to a second supply voltage source;

- a flip-flop, having a pair of inputs coupled to the clock source and the first circuit, to generate a second data signal in response to the clock signal and the first data signal;

- a first level shifter, coupled to the ~~first circuit~~flip-flop, to generate a level shifted data signal in response to the [[first]]second data signal[[; and]]

- a delay element coupled to the clock source and responsive to the clock signal to generate a delayed clock signal having a triggering clock edge; and

- a downstream latch, having an open state and a close state, a pair of inputs coupled to the first level shifter and the ~~clock source~~delay element and an output coupled to the second circuit, to generate an output data signal in response to the level shifted data signal and the delayed clock signal, with the triggering clock edge of the delayed clock signal switching the downstream latch from the close state to the open state.

2. (Currrently Amended) The apparatus according to claim 1, further comprising:

- a second level shifter, coupled between the clock source and the downstream latch and in series with the delay element~~, to generate a level shifted clock signal in response to the clock signal; and~~

~~- the downstream latch, having the pair of inputs coupled to the first level shifter and the second level shifter, to generate the output data signal in response to the level shifted data signal and the level shifted clock signal~~.

3. (Currently Amended) The apparatus according to claim 2, wherein the ~~level shifted~~delayed clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; ~~the downstream latch has an open and a close state; and the downstream latch is switched from the close state to open state by a~~ and the triggering clock edge is selected from the rising clock edge and the falling clock edge.

4. (Currently Amended) The apparatus according to claim [[2]]1, wherein the [[level shifted]] delayed clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; ~~the downstream latch has an open and a close state;~~ and the downstream latch is switched from the close state to the open state by [[a]] the triggering clock edge selected from the rising clock edge and the falling clock edge and switched from the open state to [[a]]the close state by the non-selected clock edge of the rising clock edge and the falling clock edge.

5. (Canceled)

6. (Currently Amended) The apparatus according to claim [[5]]4, wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to delay an arrival of the triggering clock edge at the downstream latch until after an arrival of the rising and falling data edges at the ~~second level shifter~~downstream latch.

7. (Currently Amended) The apparatus according to claim [[5]]4, wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to introduce a predetermined delay having a duration exceeding a time period during which the rising and falling data edges are mismatched.

8. (Currently Amended) The apparatus according to claim 6, ~~further comprising:~~

~~- a flip-flop, coupled to the first circuit, including~~ wherein the flip-flop includes a master latch coupled to the clock source and an upstream slave latch, having inputs coupled to the master latch and the clock source and an output coupled to the first level shifte[[d]]r, to generate the [[first]]second data signal; and wherein the downstream latch is a downstream slave latch.

9. (Currently Amended) The apparatus according to claim 8, wherein ~~the first circuit generates an input signal;~~ the master latch has an input to receive the ~~input~~first data signal; and the flip-flop is operable to generate the ~~first~~second data signal in response to the ~~input~~first data signal.

10. (Currently Amended) An apparatus, comprising:

- a microprocessor including a central processing unit (CPU) section having a first supply voltage source; an input-output (I/O) section having a second supply voltage source; a clock source to generate a clock signal; and a selected section of the CPU section and the I/O sections being operable to generate a first data signal, with the selected section providing a first data signal;

- a converter circuit including a flip-flop, coupled to the clock source and the selected section, to generate a second data signal in response to the clock signal and the first data signal; a first level shifter, coupled to the selected section, to generate a level shifted data signal in response to the [[first]]second data signal; a delay element and a second level shifter, coupled in series to the clock source, to generate a level shifted clock signal with a triggering clock edge in response to the clock signal; [[and]] a downstream latch[[,]] having an open and a close state, a pair of inputs coupled to the first ~~and second~~ level shifter[[s]] and the series-coupled delay element and second level shifter, and an output coupled to the non-selected section of the CPU and I/O sections[[,]]; the downstream latch adapted to generate an output data signal in response to the level shifted data signal and the triggering clock edge of the level shifted clock signal.

11. (Currently Amended) The apparatus according to claim 10, wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; the downstream latch has an open and a close state; and the downstream latch is switched from the close state to the open state by [[a]]the triggering clock edge selected from the rising clock edge and the falling clock edge.

12. (Canceled)

13. (Currently Amended) The apparatus according to claim [[12]]11, wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is operable to delay an arrival of the triggering clock edge at the downstream latch until after an arrival of the rising and falling data edges at the ~~second level shifter~~downstream latch.

14. (Currently Amended) The apparatus according to claim 13, wherein ~~the converter circuit includes a~~ the flip-flop ~~having~~includes a master latch coupled to the clock source and an upstream slave latch, having inputs coupled to the master latch and the clock source and an output coupled to the first level shifte[[d]]r, to generate the [[first]]second data signal; and the downstream latch being a downstream slave latch.

15. (Currently Amended) The apparatus according to claim 14, wherein ~~the selected section generates an input signal;~~ the master latch has an input to receive the ~~input~~ first data signal; and the flip-flop is operable to generate the ~~first~~second data signal in response to the ~~input~~first data signal.

16. (Currently Amended) A system, comprising:

- a microprocessor including a central processing unit (CPU) section coupled to a first supply voltage source; an input-output (I/O) section coupled to a second supply

voltage source; a clock source to generate a clock signal; and the CPU section being operable to generate a first data signal;

- a converter circuit including a flip-flop, coupled to the clock source and the selected section, to generate a second data signal in response to the clock signal and the first data signal; a first level shifter, coupled to the CPU section, to generate a level shifted data signal in response to the [[first]]second data signal; a delay element and a second level shifter, coupled in series to the clock source, to generate a level shifted clock signal having a triggering clock edge in response to the clock signal; and a downstream latch[[,]] having an open and a close state, a pair of inputs coupled to the first and second level shifters and an output coupled to the I/O section[[,]]; the downstream latch being adapted to generate an output data signal in response to the level shifted data signal and the triggering clock edge of the level shifted clock signal;

- a source synchronous bus, coupled to the I/O section, to receive the level shifted data signal and the level shifted clock signal; and

- an I/O module coupled to the source synchronous bus.

17. (Original) The system according to claim 16, wherein the I/O module is a selected one of a graphics and a video controller.

18. (Currrently Amended) The system according to claim 16, wherein the level shifted clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; the downstream latch has an open and a close state; and the downstream latch is switched from the close state to open state by [[a]]the triggering clock edge selected from the rising clock edge and the falling clock edge.

19. (Canceled)

20. (Currently Amended) The system according to claim 19, wherein the level shifted data signal has a plurality of rising and falling data edges and the delay element is

operable to delay an arrival of the triggering clock edge until after an arrival of the rising and falling data edges at the ~~second level shifter~~downstream latch.

21. (Currently Amended) The system according to claim 20, wherein ~~the converter circuit includes a flip-flop having~~the fiip-flop includes a master latch coupled to the clock source and an upstream slave latch, having inputs coupled to the master latch and the clock source and an output coupled to the first level shifte[[d]]r, to generate the [[first]]second data signal; and the downstream latch being a downstream slave latch.

22. (Currently Amended) The system according to claim 21, wherein ~~the CPU section generates an input signal;~~ the master latch has an input to receive the ~~input~~first data signal; and the flip-flop is operable to generate the [[first]]second data signal in response to the [[input]]first data signal.

23. (Canceled)

24. (Canceled)

25. (Canceled)

26. (Canceled)

27. (Canceled)

28. (New) A converter circuit, comprising

- a flip-flop including a master latch and an upstream slave latch, to generate a latched data signal in response to a clock signal and an input data signal;

- a first level shifter, coupled to the flip-flop, to generate a level shifted data signal in response to the latch data signal, with the level shifted data signal having a plurality of signal transistions;

- a delay element to generate a delayed clock signal having a triggering clock edge in response to the clock signal; and

- a downstream slave latch having an open and a close state, coupled to the first level shifter and the delay element, to generate an output data signal in response to the level shifted data signal and the triggering clock edge.

29. (New) The converter circuit according to claim 28, wherein the delay element is adapted to delay an arrival of the triggering clock edge at the downstream slave latch until after an arrival of the signal transitions at the downstream slave latch.

30. (New) The converter circuit according to claim 29, further comprising:

- a second level shifter, coupled in series with the delay element, to voltage level shift the delayed clock signal.

31. (New) The converter circuit according to claim 30, wherein the delayed clock signal has a plurality of clock cycles with each of the clock cycles having a rising clock edge and a falling clock edge; and the downstream latch is switched from the close state to open state by the triggering clock edge, with the triggering clock edge being selected from the rising clock edge and the falling clock edge.

32. (New) The converter circuit, according to claim 28, further comprising

- a second level shifter, coupled in series with the delay element, to voltage level shift the delayed clock signal: and

wherein the the delay element is adapted to introduce a predetermined delay having a duration exceeding a time period during which the rising and falling data edges are mismatched.